



C PAI 25-12

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FIG. 1

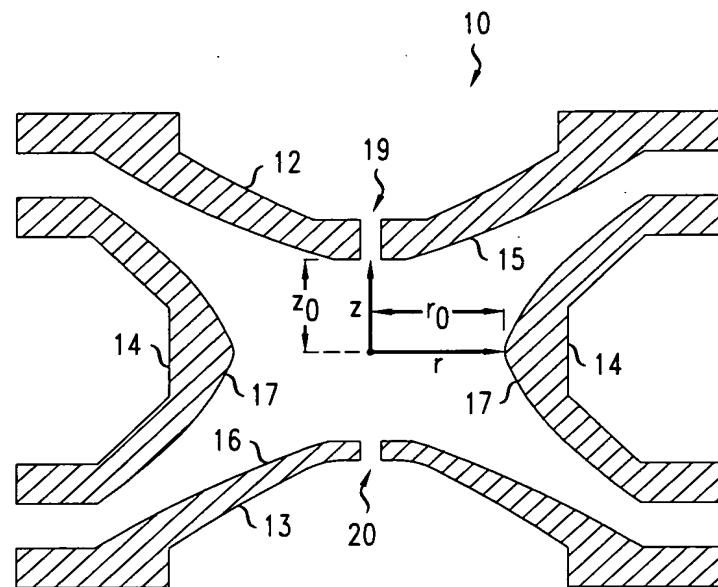
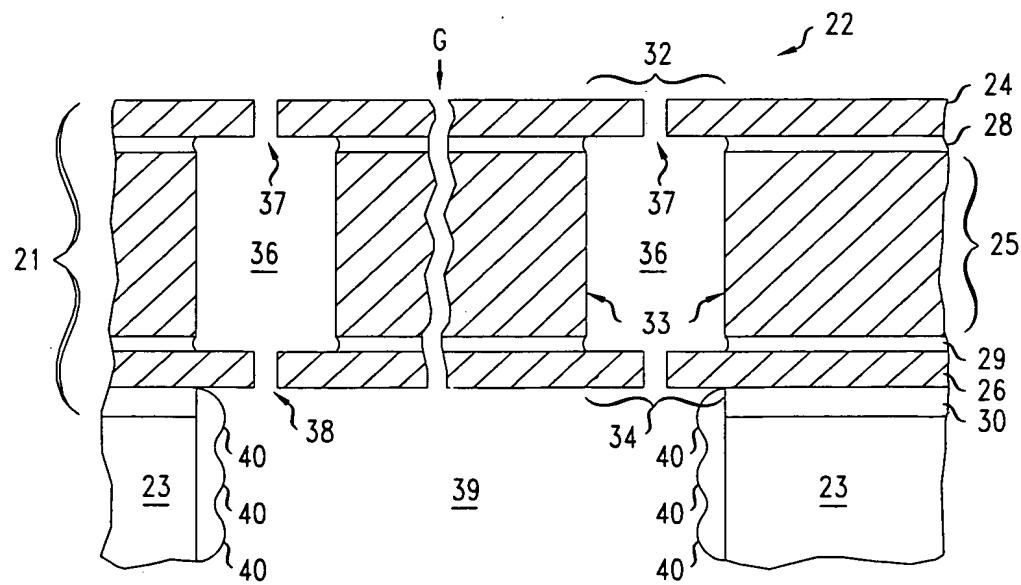


FIG. 2A



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FIG. 2B

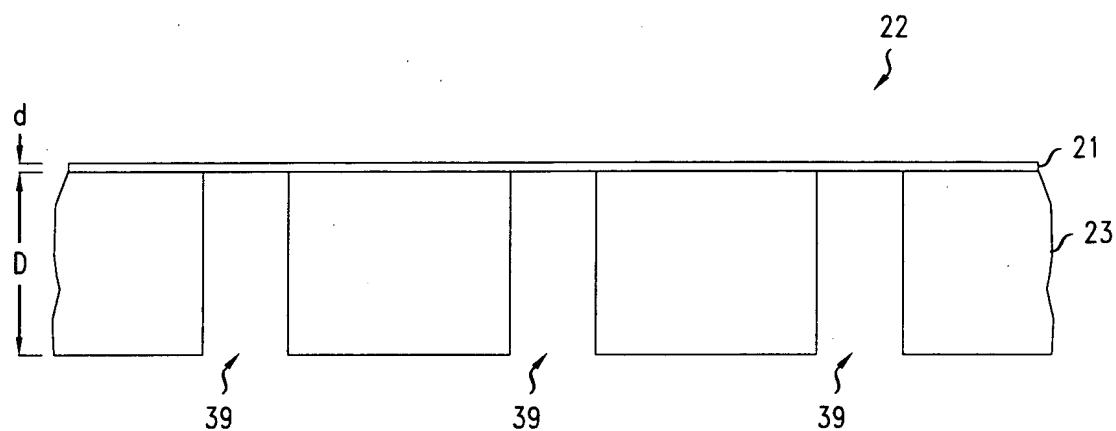
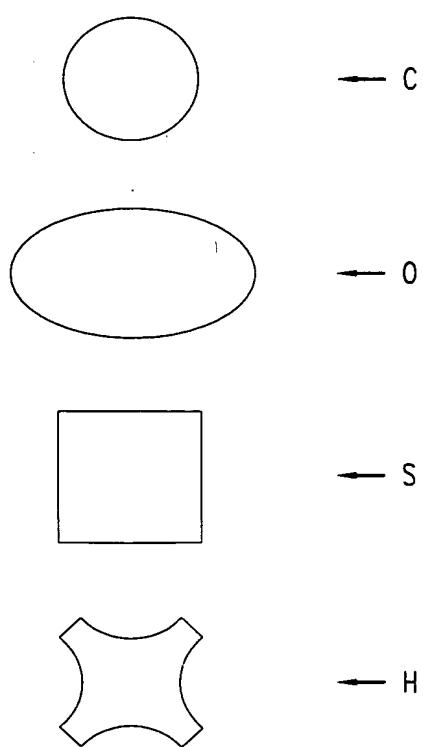


FIG. 2C



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FIG. 3

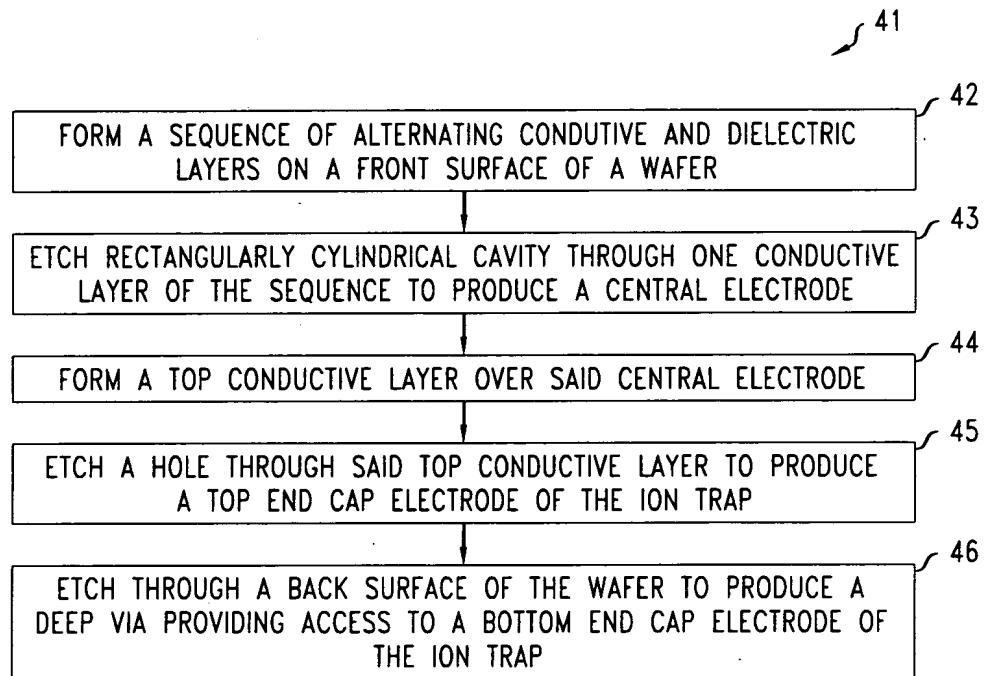
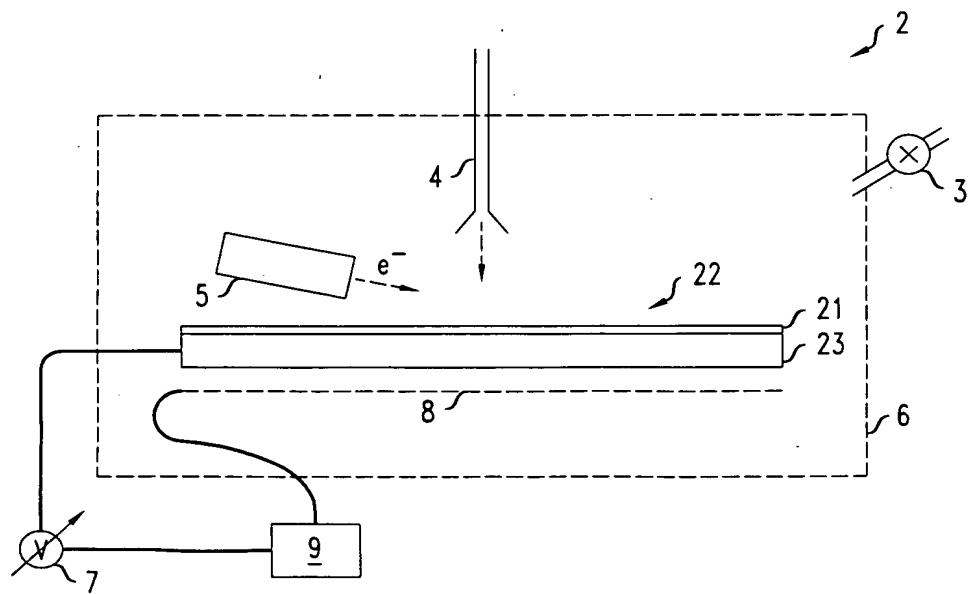


FIG. 4



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FIG. 5

- 50
- 51  
PERFORM DEPOSITIONS TO FORM A SEQUENCE THAT INCLUDES AN AI LAYER AND DIELECTRIC LAYERS AND ETCH THE AI LATER TO COMPLETE THE TRAPS' BOTTOM END CAP ELECTRODES
- 52  
DEPOSIT A SECOND AI LAYER FOR THE TRAPS' CENTRAL ELECTRODES
- 53  
DRY ETCH THE SECOND AI LAYER TO FORM TRAPPING CAVITIES AND COMPLETE THE CENTRAL ELECTRODES
- 54  
DEPOSIT SACRIFICIAL AMORPHOUS SILICON TO FILL THE CAVITIES IN THE CENTRAL ELECTRODES
- 55  
CMP THE SACRIFICIAL LAYER OF AMORPHOUS SILICON TO PRODUCE A FLAT TOP SURFACE
- 56  
DEPOSIT A THIRD AI LAYER FOR THE TRAPS' TOP END CAP ELECTRODES ON THE FLAT TOP SURFACE
- 57  
DRY ETCH THE THIRD AI LAYER TO COMPLETE THE TOP END CAP ELECTRODES AND REMOVE EXPOSED OXIDE
- 58  
DEPOSIT PROTECTIVE LAYER OVER STRUCTURE ON FRONT SURFACE OF WAFER
- 59  
MECHANICAL GRIND BACKSIDE OF THE WAFER TO CONVENIENT THICKNESS
- 60  
PERFORM DEEP ETCH VIA THROUGH BACK SURFACE OF WAFER TO EXPOSE BOTTOM END CAP ELECTRODE
- 61  
PERFORM ETCH TO REMOVE SACRIFICIAL MATERIAL FROM THE TRAPPING CAVITIES AND PORTS THERETO

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FIG. 6

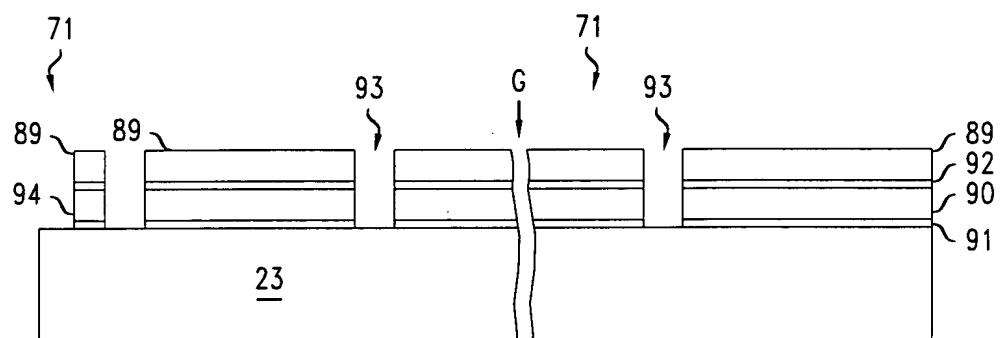
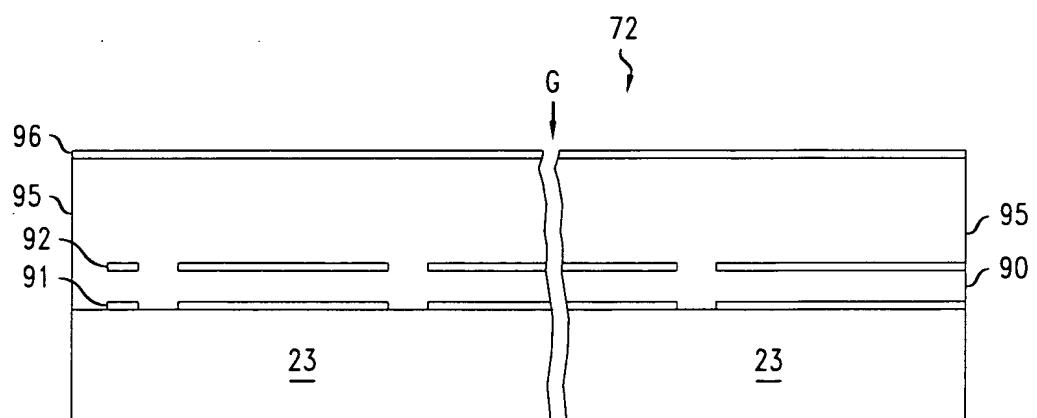


FIG. 7



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FIG. 8

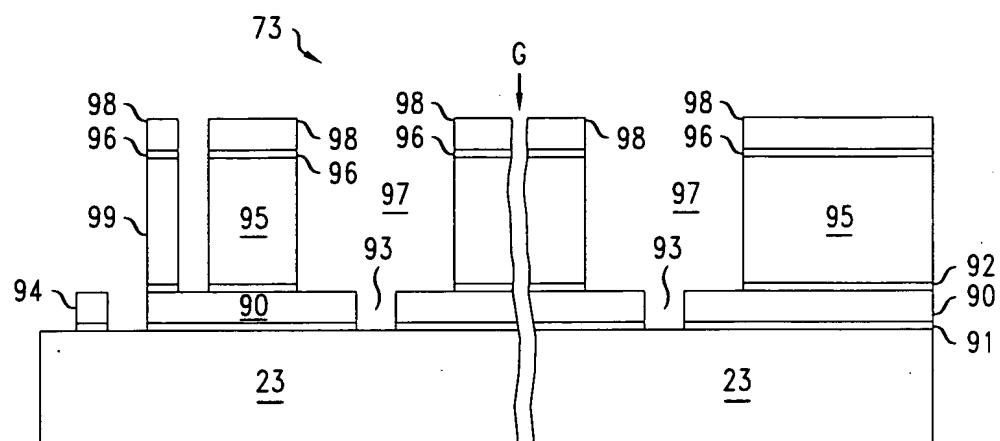
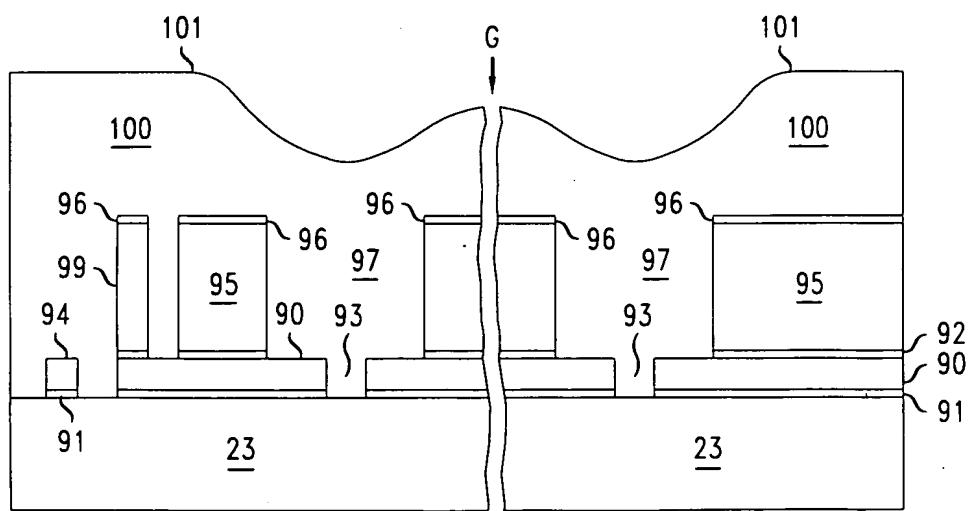


FIG. 9



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FIG. 10

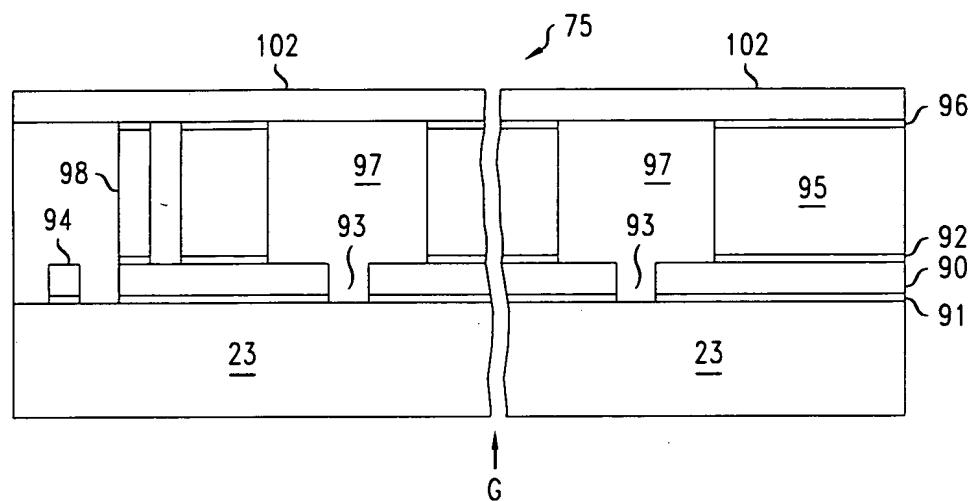
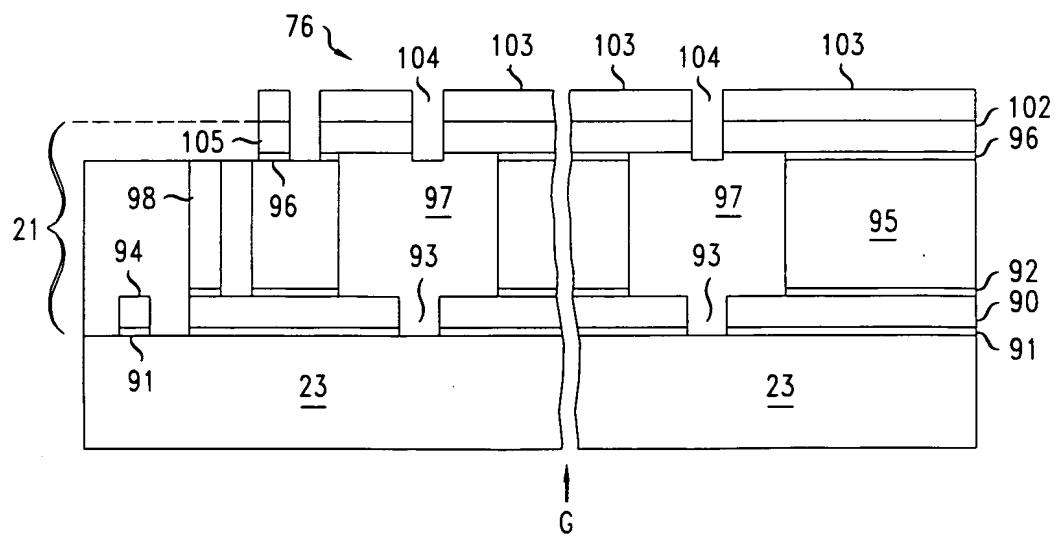


FIG. 11



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FIG. 12

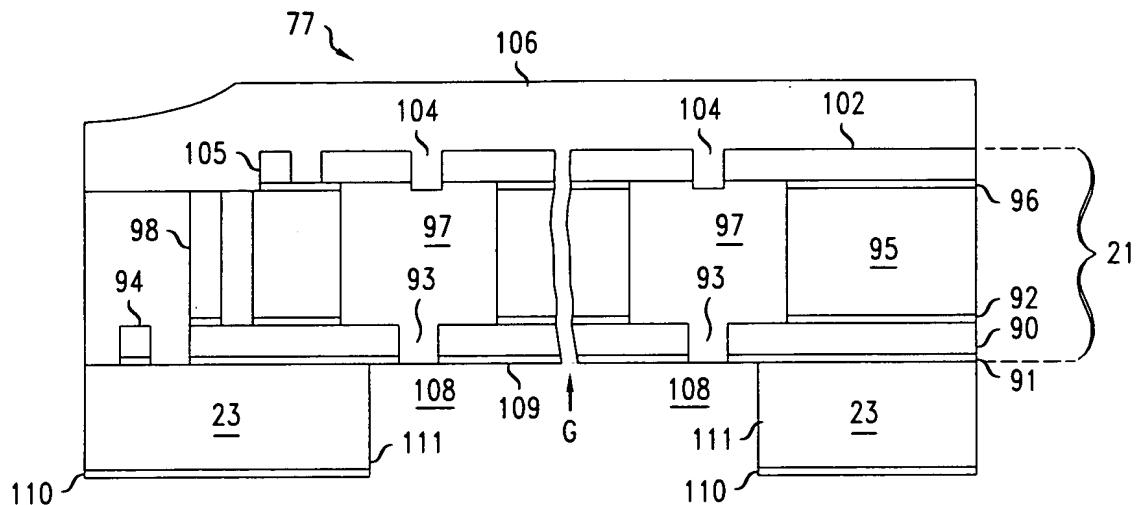


FIG. 13

